Power report

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| Xilinx XPower Analyzer |

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| Release | 14.7 - P.20131013 (nt64) |

| Command Line | Generated from Graphical User Interface |

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1. Settings

1.1. Project

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| Project |

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| Design File | WS.ncd |

| Settings File | NA |

| Physical Constraints File | WS.pcf |

| Simulation Activity File | NA |

| Design Nets Matched | NA |

| Simulation Nets Matched | NA |

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1.2. Device

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| Device |

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| Family | Artix7 |

| Part | xa7a100t |

| Package | csg324 |

| Temp Grade | Industrial |

| Process | Typical |

| Speed Grade | -2I |

| Characterization | Preliminary,v1.0,2012-07-11 |

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1.3. Environment

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| Environment |

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| Ambient Temp (C) | 25.0 |

| Use custom TJA? | No |

| Custom TJA (C/W) | NA |

| Airflow (LFM) | 250 |

| Heat Sink | Medium Profile |

| Custom TSA (C/W) | NA |

| Board Selection | Medium (10"x10") |

| # of Board Layers | 12 to 15 |

| Custom TJB (C/W) | NA |

| Board Temperature (C) | NA |

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1.4. Default Activity Rates

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| Default Activity Rates |

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| FF Toggle Rate (%) | 12.5 |

| I/O Toggle Rate (%) | 12.5 |

| Output Load (pF) | 5.0 |

| I/O Enable Rate (%) | 100.0 |

| BRAM Write Rate (%) | 50.0 |

| BRAM Enable Rate (%) | 50.0 |

| DSP Toggle Rate (%) | 12.5 |

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2. Summary

2.1. On-Chip Power Summary

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| On-Chip Power Summary |

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| On-Chip | Power (mW) | Used | Available | Utilization (%) |

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| Clocks | 0.00 | 1 | --- | --- |

| Logic | 0.00 | 2 | 63400 | 0 |

| Signals | 0.00 | 8 | --- | --- |

| IOs | 0.00 | 21 | 210 | 10 |

| Static Power | 82.16 | | | |

| Total | 82.16 | | | |

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2.2. Thermal Summary

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| Thermal Summary |

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| Effective TJA (C/W) | 4.6 |

| Max Ambient (C) | 99.6 |

| Junction Temp (C) | 25.4 |

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2.3. Power Supply Summary

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| Power Supply Summary |

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| | Total | Dynamic | Static Power |

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| Supply Power (mW) | 82.16 | 0.00 | 82.16 |

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| Power Supply Currents |

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| Supply Source | Supply Voltage | Total Current (mA) | Dynamic Current (mA) | Quiescent Current (mA) |

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| Vccint | 1.000 | 16.74 | 0.00 | 16.74 |

| Vccaux | 1.800 | 13.15 | 0.00 | 13.15 |

| Vcco18 | 1.800 | 4.00 | 0.00 | 4.00 |

| Vccbram | 1.000 | 0.35 | 0.00 | 0.35 |

| Vccadc | 1.710 | 20.00 | 0.00 | 20.00 |

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2.4. Confidence Level

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| Confidence Level |

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| User Input Data | Confidence | Details | Action |

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| Design implementation state | High | Design is completely routed | |

| Clock nodes activity | High | User specified more than 95% of clocks | |

| I/O nodes activity | High | User specified more than 95% of inputs | |

| Internal nodes activity | High | User specified more than 25% of internal nodes | |

| Device models | Medium | Device models are not Production | Device models may change and in turn slightly affect accuracy |

| | | | |

| Overall confidence level | High | | |

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3. Details

3.1. By Hierarchy

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| By Hierarchy | Power (mW) | Logic Power (mW) | Signal Power (mW) | # FFs | # LUTs |

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| Hierarchy total | 0.00 | 0.00 | 0.00 | 1 | 2 |

| WS | 0.00 | 0.00 | 0.00 | 1 | 2 |

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3.2. By Clock Domain

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| By Clock Domain : 1 | Power (mW) | Freq (MHz) | Buffer | Buffer Enable (%) | Enable Signal | Fanout | Slice Fanout |

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| clock\_BUFGP/IBUFG | | | | | | | |

| Logic: | | | | | | | |

| clock\_BUFGP/BUFG | 0.00 | 0.00 | BUFG | NA | NA | NA | NA |

| Nets: | | | | | | | |

| clock\_BUFGP | 0.00 | 0.00 | BUFG | NA | NA | 1 | 1 |

| clock\_BUFGP/IBUFG | 0.00 | 0.00 | NA | NA | NA | 1 | 1 |

| | | | | | | | |

| Total | 0.00 | | | | | | |

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3.3. By Resource Type

3.3.1. Core Dynamic

3.3.1.1. Logic

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| Logic | Power (mW) | Type | Clock (MHz) | Clock Name | Signal Rate |

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| S<0>1 | 0.00 | LUT6 | Async | Async | 0.0 |

| ps | 0.00 | FF | 0.0 | clock\_BUFGP | 0.0 |

| sev/\_n00071 | 0.00 | LUT6 | Async | Async | 0.0 |

| | | | | | |

| Total | 0.00 | | | | |

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3.3.1.2. Signals

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| Signals | Power (mW) | Signal Rate | % High | Fanout | Slice Fanout | Clock | Logic Type |

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| lightOut\_OBUF | 0.00 | 0.00 | 50.0 | 3 | 3 | Async | NA |

| moistOut\_0\_OBUF | 0.00 | 0.00 | 50.0 | 3 | 3 | Async | NA |

| moistOut\_1\_OBUF | 0.00 | 0.00 | 50.0 | 3 | 3 | Async | NA |

| moistOut\_2\_OBUF | 0.00 | 0.00 | 50.0 | 3 | 3 | Async | NA |

| mySeg\_1\_OBUF | 0.00 | 0.00 | 65.5 | 4 | 4 | Async | NA |

| ps | 0.00 | 0.00 | 17.5 | 3 | 3 | clock\_BUFGP | NA |

| reset\_IBUF | 0.00 | 0.00 | 1.0 | 1 | 1 | Async | NA |

| tempOut\_OBUF | 0.00 | 0.00 | 50.0 | 3 | 3 | Async | NA |

| | | | | | | | |

| Total | 0.00 | | | | | | |

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3.3.2. IO

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| IO | Power (mW) | I/O Standard | Signal Rate | % High | Clock (MHz) | Clock Name | Input Pins | Output Pins | Bidir Pins | Output Enable (%) | Output Load (pF) | Data Rate | IO LOGIC SERDES | IO DELAY | IBUF LOW PWR | Vccint (mW) | Vccaux (mW) | Vccaux\_io (mW) | Vcco On-Chip Termal (mW) | Vcco Supply Current (mA) |

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| clock | 0.00 | LVCMOS18 | 0.00 | 50.0 | Async | Async | 1 | 0 | 0 | NA | 0 | Async | No | Off | Yes | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| light | 0.00 | LVCMOS18 | 0.00 | 50.0 | Async | Async | 1 | 0 | 0 | NA | 0 | Async | No | Off | Yes | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| lightOut | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 50.0 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| moist<0> | 0.00 | LVCMOS18 | 0.00 | 50.0 | Async | Async | 1 | 0 | 0 | NA | 0 | Async | No | Off | Yes | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| moist<1> | 0.00 | LVCMOS18 | 0.00 | 50.0 | Async | Async | 1 | 0 | 0 | NA | 0 | Async | No | Off | Yes | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| moist<2> | 0.00 | LVCMOS18 | 0.00 | 50.0 | Async | Async | 1 | 0 | 0 | NA | 0 | Async | No | Off | Yes | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| moistOut<0> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 50.0 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| moistOut<1> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 50.0 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| moistOut<2> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 50.0 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| mySeg<0> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 0.0 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| mySeg<1> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 65.5 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| mySeg<2> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 65.5 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| mySeg<3> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 100.0 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| mySeg<4> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 65.5 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| mySeg<5> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 65.5 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| mySeg<6> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 100.0 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| myState<0> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 17.5 | 0.00 | clock\_BUFGP | 0 | 1 | 0 | NA | 5 | SDR | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| myState<1> | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 0.0 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| reset | 0.00 | LVCMOS18 | 0.00 | 1.0 | Async | Async | 1 | 0 | 0 | NA | 0 | Async | No | Off | Yes | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| temp | 0.00 | LVCMOS18 | 0.00 | 50.0 | Async | Async | 1 | 0 | 0 | NA | 0 | Async | No | Off | Yes | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| tempOut | 0.00 | LVCMOS18\_12\_SLOW | 0.00 | 50.0 | Async | Async | 0 | 1 | 0 | NA | 5 | Async | No | Off | No | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |

| | | | | | | | | | | | | | | | | | | | | |

| Internal VREFs (0) | 0.00 | | | | | | | | | | | | | | | | | | | |

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| Total | 0.00 | | | | | | | | | | | | | | | | | | | |

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4. Warnings

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WARNING:Power:1337 - Clock frequency for clock net "clock\_BUFGP" is zero.

WARNING:Power:1337 - Clock frequency for clock net "clock\_BUFGP/IBUFG" is zero.

WARNING:Power:1369 - Clock frequency for one or more clocks was not found through

timing constraints (PCF file) or simulation data. Without knowing the

clock frequency of all clocks, dynamic power information for those clock

domains will default to zero which may under-estimate the power for this

design. To avoid this warning, provide at least one of the following:

1. The proper timing constraints (PERIOD) for clocks (re-implement design

and load the newly generated PCF file into XPower Analyzer)

2. A post PAR simulation-generated VCD or SAIF file indicating clock

frequencies

3. The clock frequency for clocks in the "By Type -> Clocks" view in the

XPower Analyzer GUI and then applying "Update Power Analysis"

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Analysis completed: Sat Jul 09 17:39:14 2022

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